AUTOMATED DESIGN-AWARE OPTIMIZED FILL METHODOLOGY

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Motivation:
Optimize fill without impacting design performance and reliability

- Whether performed by designers or foundries, metal fill insertion is mandatory at advanced nodes to ensure manufacturability and high yield
- Manual identification of critical design elements (nets/devices) is time-consuming, resource-intensive, and non-scalable
- Metal fill affects timing due to added capacitance. Balancing density requirements with timing on critical nets is crucial for both timely design closure and design reliability
- Fill consistency is required for sensitive nets and devices
  (e.g., RF/analog designs are sensitive to parasitic coupling between signals and fill)

Need:
Automated methodology that can link design awareness with optimized geometrical fill insertion to protect critical/sensitive nets and devices

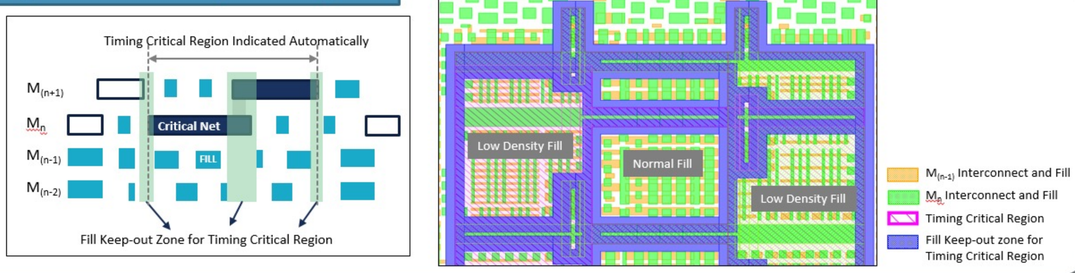
1. Re-use the output database created in the layout-vs-schematic (LVS) run*
2. Identify critical nets in the design layout netlist using designer-defined criteria**
3. Find corresponding geometries in the design layout
4. Generate geometrical marker layers for these critical nets in GDS/OASIS format
5. Merge the markers GDS/OASIS database with design GDS/OASIS database to capture target design nets that overlap for special spacing constraints consideration during fill shape generation
6. Insert optimized fill
7. Simulate the design with optimized fill shapes insertion

* Reusing database from LVS run eliminates need to re-extract the layout to get the design layout netlist required to capture critical nets

** Name or connectivity to specified device types or circuit structures. These criteria are coded into a circuit reliability verification tool (e.g., the Calibre® PERC™ reliability platform)

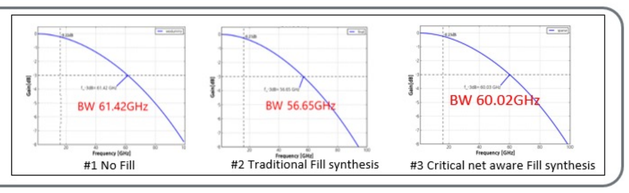
Results:
Proposed flow provides significant benefit on high-speed IPs by minimizing the parasitic capacitance increase due to fill patterns

Diagram & Fill Patterns of Optimized Fill Synthesis



Total capacitance & Simulation results

Fill Synthesis	*Total Cap. (fF)*	*Total Cap. Reduction*
No Fill	33.19	-
Traditional Fill Synthesis	47.49	1x
Critical net aware Fill synthesis	37.73	0.79x



- Increase in total capacitance reduced ~20.55%
- Simulation showed improved performance compared to traditional fill synthesis
- Reuse of LVS database reduced design turnaround time while maintaining connectivity consistency between components